A New Resonant Modular Multilevel Step-Down DC–DC Converter with Inherent-Balancing

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***Abstract*—Modular multilevel converters (MMCs) have become increasingly interesting in dc–dc applications, as there is a growing demand for dc–dc converters in high-voltage applications. Power electronics transformers can be used for high step-down ratio dc–dc power conversion, with high power rating and efficiency achieved. However, this arrangement requires a large number of high isolation voltage transformers and a complicated balancing control scheme. To provide a simple solution with inherent voltage balancing, this paper presents a new resonant MMC topology for dc–dc conversion. The proposed converter achieves high-voltage step-down ratio depending on the number of submodules. The converter also exhibits simplicity and scalability with no necessary requirement of high-voltage isolation transformers. By using phase-shift control, a much higher converter operating frequency is achieved compared to the switching frequency. Resonant conversion is achieved between the series inductor and submodule capacitors. The operation principle and theoretical analysis are presented in this paper, which have been verified by experimental results based on a bench-scale prototype.**

***Index Terms*—DC–DC conversion, modular multilevel converters (MMCs), phase-shift control, resonant converter, step-down ratio.**

I. Introduction

MODULAR multilevel converters (MMCs) are used for dc–ac [1]–[5], ac–dc [4], [6]–[8], ac–ac [9], [10], and dc–dc [11]–[13] conversion for medium-voltage and high-voltage applications. These converters provide more than two levels which can be adjusted by changing the number of modular cells. Cells with a fault can also be bypassed while keeping the converters operating. High reliability and modularity are the main features of MMCs. However, all these MMCs require a complicated balancing control to maintain the voltage levels. Even though a requirement is placed on the tolerance of the cell capacitors, measuring capacitor voltages for balancing control is indispensable. Moreover, the operating frequency of the conventional control for MMCs is not higher than the switching frequency. High switching frequencies are used to reduce the sizes of passive components. Tradeoffs between switch ratings and converter size should be made, but it is hard to find a good solution for high-voltage, high-step-down ratio, and low-power applications.

Manuscript received August 21, 2013; revised October 30, 2013 and December 28, 2013; accepted January 16, 2014. Date of publication January 22, 2014; date of current version August 26, 2014. This work was supported by the Engineering and Physical Sciences Research Council under Grant EP/K006312/1. Recommended for publication by Associate Editor M. A. Perez.

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Digital Object Identifier 10.1109/TPEL.2014.2301974

Other new multilevel modular switched capacitor dc–dc converters designed for small-power applications are proposed in [14]–[16]. These converters exhibit good efficiency and modularity, but are not suitable for high-voltage applications. For high-voltage applications, conventional diode clamped, flying capacitor, or other types of converters are also not suitable as the circuit configuration becomes quite complicated with increased number of levels [17], [18]. These converters have poor modularity and reliability. The most promising solution may be converters known as power electronics transformers (PETs) [11], [12], [19], [20]. PETs are designed for high-power applications. They require a large number of transformers with high-voltage isolation. The isolation between the primary side and secondary side has to withstand the entire high input voltage, even if the voltage across the primary side is only a small fraction of this. The secondary side terminals of the transformers are connected in parallel, and the balancing control between modules is necessary. PETs can be used for high-voltage and high-power applications with high efficiency, but the converter size will be increased dramatically with a high-voltage step-down ratio. Therefore, other simple solutions may be promising for low-power applications in medium-voltage and high-voltage applications.

This paper presents a new form of MMC for high-voltage step-down unidirectional dc–dc conversion [13]. The proposed converter has inherent-balancing of each capacitor voltage. High step-down voltage conversion ratios can be achieved by using large numbers of submodules. With phase-shifted pulse width-modulation (PWM), higher operating frequency can also be achieved, which is equivalent to the product of the number of submodules and the switching frequency. Moreover, the converter operates with two resonant frequencies where zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) become possible. The proposed converters are more suitable for low-power dc–dc applications as it has the feature of modularity, simplicity, and flexibility. The detailed configuration and operation principle are presented, and verified by experimental results from bench-scale prototype tests.

II. High Step-Down Ratio DC–DC Converters and General Operating Principle

A. System Configuration

In [13], a family of dc–dc converters are discussed in which three groups of submodules are used as two voltage dividers, and passive filters are provided at input and outputs connections to pass and block currents of appropriate frequencies [13, Fig. 5(b)]. On the right-half-hand side of the circuit in [13, Fig. 5(b)], one load is fed by one group of submodules.

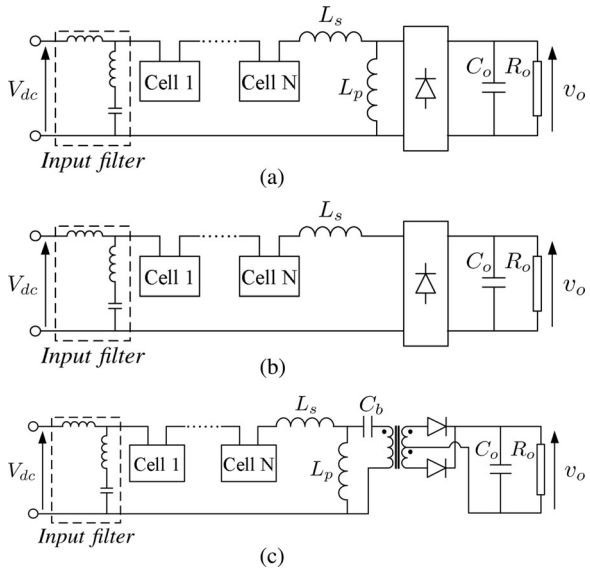

Fig. 1. High step-down ratio unidirectional dc–dc converter topologies. (a) Transformerless converter with series–parallel resonance. (b) Transformerless converter with series resonance. (c) Transformer isolated converter.

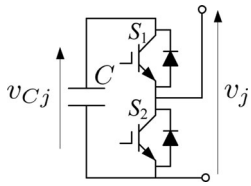

Fig. 2. Circuit configuration of a half-bridge cell.

Here, the proposal is also to use only one group of submodules in the upper position to support the dc-voltage difference between the input and output but also provide excitation to a resonant output stage connected to the return terminal of the input. Fig. 1(a) and (b) shows series–parallel [21]–[24] and series [25], [26] resonant versions in which the resonance is between the series inductors and the submodule capacitors. The submodules are illustrated in Fig. 2. The output rectifier can be coupled via a transformer but only by adding a capacitor to block the dc current as shown in Fig. 1(c). For the circuits of Fig. 1(a) and (c), the dc current drawn from the input and through the cells returns via the parallel inductor L_p. For the circuit of Fig. 1(b), where this path is absent, the return of the dc input current is via the rectifier and load.

B. Phase-Shifted PWM for High Step-Down Ratio

To support the input voltage, the submodules of Fig. 1 are used predominantly in the "one state" in which the upper switch is ON and the module inserts the capacitor voltage into the circuit. Phase-shifted PWM is then applied with a high duty-ratio such that an excitation is applied to the resonant components. The effective frequency of this excitation is much higher than the frequency of switching of an individual cell [27], [28]. This is arranged so that only one cell at a time is in "zero state," and thus, the step-down ratio of the circuit becomes dependent on the number of cells N. To demonstrate the general operation

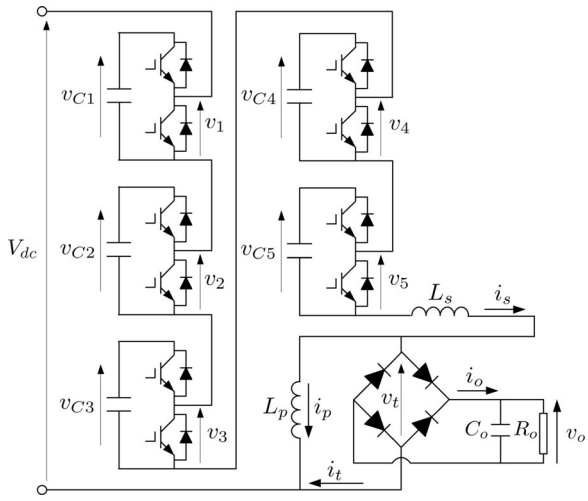

Fig. 3. Five-cell step-down series–parallel resonant converter.

principle, the converter in Fig. 1(a) with five half-bridge cells is used as an example. Fig. 3 shows the circuit diagram with the input filter removed to simplify the analysis. The dc input voltage is $V_{\rm dc}$. The capacitor voltage and output voltage of jth ($j = 1, 2, \ldots, 5$) cell are represented by v_{Cj} and v_j, respectively. The input current i_s is composed of the dc component and ac component. The dc current component returns to the converter input mainly through the parallel inductor L_s, where an ac current component mainly flows to the rectifier. The sum of the parallel inductor current i_p and the rectifier input current i_t is equal to i_s. The output current i_o is rectified from i_t. The switching frequencies and duty-ratios of cells are equal, but the PWM signals from Cell 1 to Cell 5 are shifted by 0°, 72°, 144°, 216°, and 288°, respectively. To analyze the circuit operation, the following assumptions are made:

1) The switches are lossless and the cells are identical with the same parameters.
2) The cutoff frequency of the input filter is much lower than the series current frequency in the converter. The input ac current and dc current flow through the parallel branch and the series branch of the input filter, respectively.
3) The dc voltages of the cell capacitors are balanced at a steady state.
4) The rectifier diodes are synchronously switched ON with the rectifier input voltage.

When the converter is operating at a steady state, the switching frequency is f_s and the duty-ratio of each cell is 90%. Based on the previous assumptions, the key voltage waveforms of the converter are shown in Fig. 4. With the phase-shift control, the output voltage of jth cell v_j is square wave ranging from 0 to the steady-state cell capacitor voltage v_{Cj}. Define output voltage across all the cells as $v_s = \sum_{j=1}^{N} v_j$. Therefore, v_s is ranging from the sum of four cells' capacitor voltages to the sum of five cells' capacitor voltages. As all the cell capacitor voltages are assumed to be equal to $\overline{v}_C$, the stack voltage v_s is comprised of a square wave ripple with the amplitude of $0.5\overline{v}_C$ and a dc offset of $4.5\overline{v}_C$. It can be observed from Fig. 4 that the ripple frequency is five times of the switching frequency. Assume there is no ac voltage drop across the passive components, the rectifier input

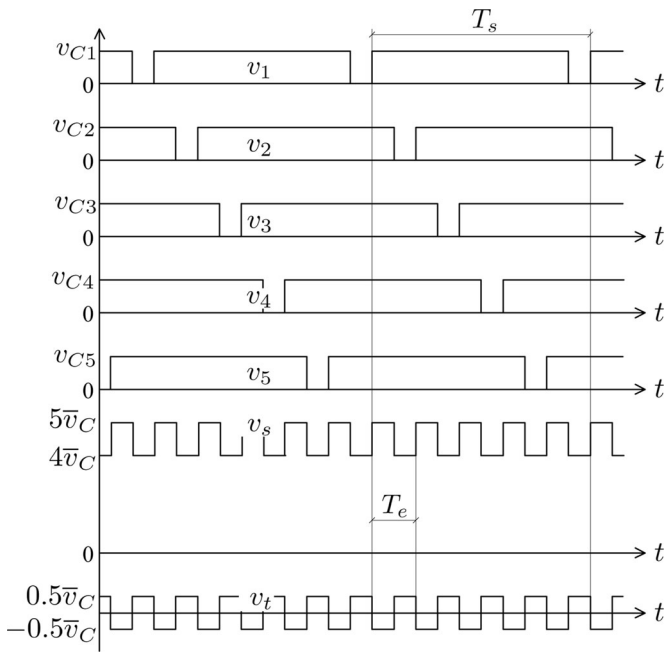

Fig. 4. Time-domain key voltage waveforms of the five-cell converter.

voltage v_t is a square wave with the amplitude of $0.5\overline{v}_C$ but in an opposite phase compared to the ripple of v_s.

As the dc offset of v_s is $4.5\overline{v}_C$ with $N = 5$, the cell capacitor voltage can be derived as $\overline{v}_C = V_{\rm dc}/4.5$. In a more general case with N cells, the average cell capacitor voltage can be derived as

$$\overline{v}_C = \frac{2V_{\rm dc}}{2N-1} \tag{1}$$

with the phase-shift angle of $\frac{360^\circ}{N}$ and the duty-ratio of $\frac{2N-1}{2N}$. Hence, the peak voltage value of v_t is $0.5\overline{v}_C$. If the converter output voltage v_o is close to the peak input voltage of the rectifier, this converter achieves a step-down ratio of $2N-1$, which is a function of the number of half-bridge cells. With more cells in the converter, higher step-down voltage ratio can be achieved.[1] The equivalent operating frequency f_e is expressed by

$$f_e = Nf_s \tag{2}$$

which is used to choose the passive components for the resonant operation.

Assume that the dc component and root mean square (RMS) value of an ac component of the series current are $I_{\rm dc}$ and $I_{\rm ac}$, respectively. If we neglect the losses of the converter, the input power is almost equal to the output power, which can be written as

$$V_{\rm dc}I_{\rm dc} = \overline{v}_o I_{\rm ac}. \tag{3}$$

As $V_{\rm dc}/\overline{v}_o = 2N-1$, it can be derived from (3) that $I_{\rm ac} = (2N-1)I_{\rm dc}$. With a rated power P, the RMS of the ac current can be derived as

$$I_{\rm ac} = (2N-1)P/V_{\rm dc}. \tag{4}$$

This means that when the output power is constant, the current RMS value and switch stress are proportional to the step-down ratio. As the ac current is usually much higher than the dc current, the conduction losses mainly come from the ac current. If we assume that the average voltages across IGBTs and diodes are the same as $V_{\rm semi}$, the conduction losses caused by the ac current can be written as

$$P_{\rm ac} = I_{\rm ac}V_{\rm semi}N. \tag{5}$$

Therefore, comparing $P_{\rm ac}$ to the input power, it can be derived that the efficiency η is limited by the conduction losses as

$$\eta < 1 - \frac{N(2N-1)V_{\rm semi}}{V_{\rm dc}}. \tag{6}$$

In most cases, if the current flowing through semiconductors is increased, the voltage drop on semiconductors increases. This gives a higher $V_{\rm semi}$ and the efficiency will reduce. As a result, the converter is only suitable for high-voltage and low-power applications. It can be seen from (6) that with a higher step-down ratio, the efficiency reduces significantly. Therefore, the step-down ratio achieved by cells should be limited. In high-voltage applications, IGBTs connected in series can also be used to construct a half-bridge. An isolation transformer can be used to further increase the step-down ratio without increasing the series ac current. Under such condition, the topology of Fig. 1(c) involving a step-down transformer becomes a good solution.

C. Resonant Operation and Inherent-Balancing

The converter family can operate in a resonant mode. The resonant operation of the converter in Fig. 1(a) is similar to that of classic series–parallel resonant converters. The operation principle of the converter in Fig. 1(b) is similar to that of series resonant converters. The resonant converter in Fig. 1(c) contains a dc-blocking capacitor and a transformer. With a relatively big capacitance C_b and magnetizing inductance of the transformer compared to that of the resonant tank, this converter can operate in a similar way to that of the converter in Fig. 1(a). This provides a further step-down voltage ratio without increasing the series current. This section presents the analysis of the equivalent operation of the first configuration (see Fig. 3). The operation principle of other configurations can be analyzed by using the similar method.

To demonstrate the operation principle in a simple way, the starting point is selected at the time when the capacitor of Cell 1 is involved into the resonant operation and the end point is selected at the time when capacitor of Cell 2 is out of the resonance. The relevant time interval can be found in Fig. 4 which is marked by the equivalent operating cycle T_e. Note that fixed dead time is used for all switches. Considering operation mode with deadband, there are four operation modes in each operating cycle, which are shown in Fig. 5.

To analyze the circuit operation, we assume the parallel current i_p is above zero. The first mode starts when the lower switch in Cell 1 is turned OFF, and the circuit enters the dead time mode

[1]The phase-shift angle is usually a fixed value but the duty-ratio can be flexible. Duty-ratios such as $\frac{2N-k}{2N}$ $(k = 1, 3, 5\ldots)$ are also applicable, resulting in lower step-down ratios such as $2N-k$. This arrangement for the converter gives the possibility of reducing the ratio of the series ac current to the dc current.

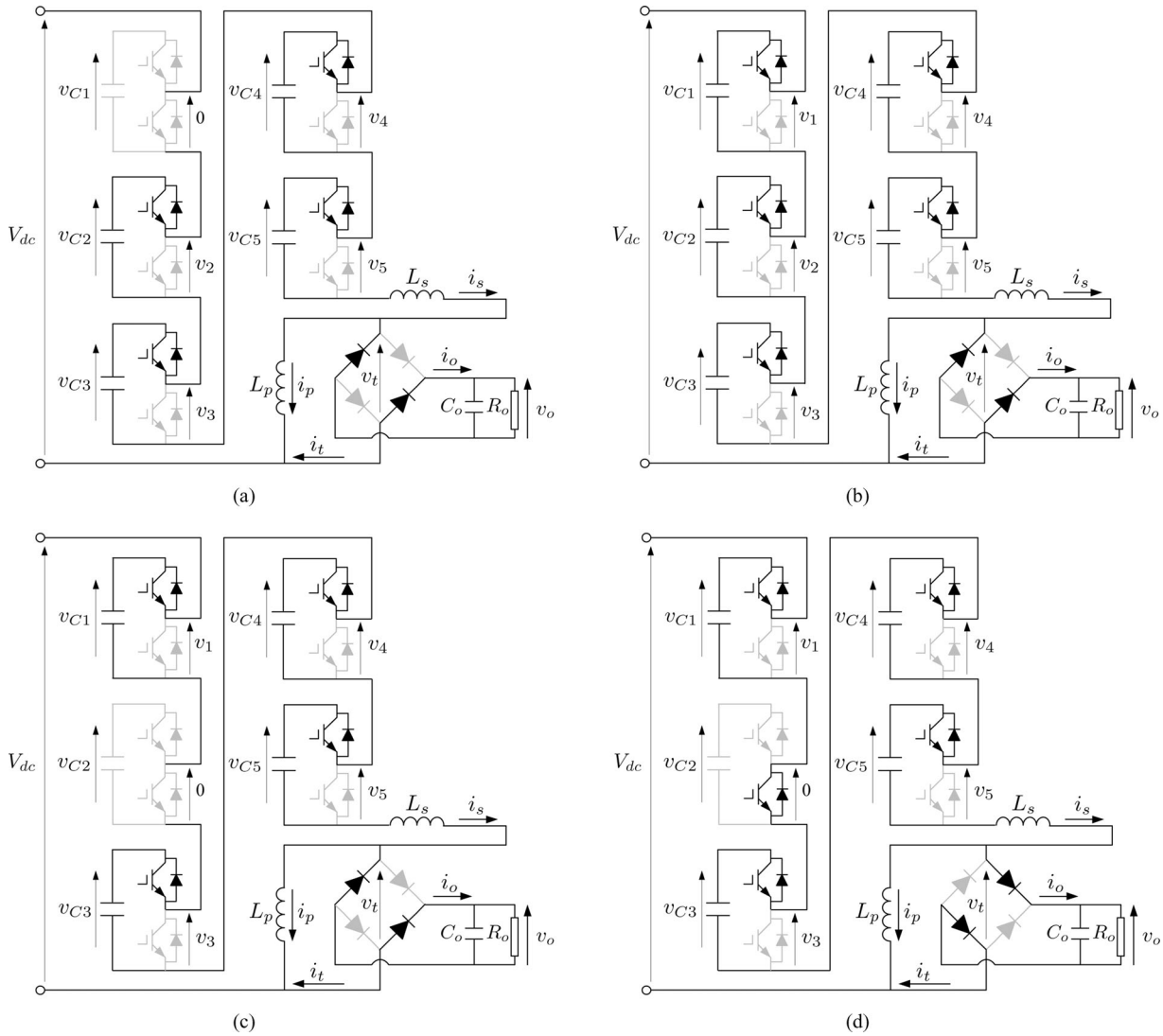

Fig. 5. Operation modes in the first equivalent operating cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (black: on path; grey: off path).

of Cell 1 [see Fig. 5(a)]. In this mode, no current flows through cells and all the current circulates between the parallel inductor and the rectifier. After a short time, the upper switch in Cell 1 is turned ON and the circuit enters mode 2 [see Fig. 5(b)]. All the cell capacitors are in series with the inductor L_s. The input voltage of the rectifier is negative. Therefore, the input current i_t is negative. This mode lasts until the upper switch of Cell 2 is turned OFF. Then, the circuit enters mode 3 [see Fig. 5(c)]. This mode is the dead time mode of Cell 2. As there is no series current, all the current on the parallel inductor flows to the diode rectifier. Shortly after that, the lower switch of Cell 2 is turned ON and the circuit becomes another resonant circuit only with capacitors of Cells 1, 3, 4, and 5 in series with L_s [see Fig. 5(d)]. As v_t becomes positive in this mode, the series current starts to rise with its resonant waveform.

In the second mode, where five capacitors are in series, the input voltage of the rectifier is negative ($v_t < 0$). With the resonant current flowing through relevant diodes, v_t is clamped by the output voltage as $v_t = -v_o$. If the output current does not fall to zero before the half T_e, the converter is operating in the continuous conduction mode (CCM). Otherwise, it may operate in the discontinuous conduction mode (DCM). When i_o falls to zero, the output is disconnected from the parallel inductor L_p and v_t is dependent on the current i_p until the next switching action occurs. On the other hand, in the last mode, one capacitor is out and four capacitors join the series resonance. The input voltage of the rectifier is clamped as $v_t = v_o$ as long as the converter operates in the CCM. If i_o falls to zero before this half operating cycle, the operation mode becomes the DCM and $i_s = i_p$ until the end of this operating cycle.

In the next cycle T_e, the capacitor of Cell 2 will be in, and later on, the capacitor of Cell 3 will be out. The following capacitors' in and out sequence should be the capacitors of Cell 3 and Cell 4, the capacitors of Cell 4 and Cell 5, the capacitors of Cell 5 and Cell 1, and finally back to the capacitors of Cell 1 and Cell 2 in the next switching cycle. Hence, there are always five capacitors or four capacitors in the series resonant operation alternatively, with the duration of each mode as half T_e. The total voltage on the series capacitors is always clamped through the diode bridge by the constant output voltage and the input voltage.

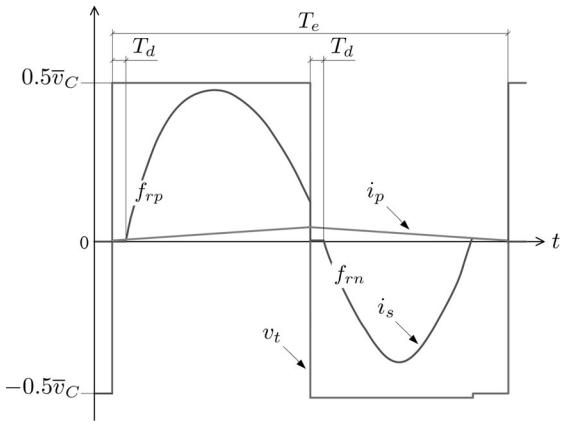

Fig. 6. Time-domain waveforms of the resonant tank.

Therefore, the dc voltages of all the capacitors should be equal in the steady state. This gives the inherent-balancing ability of the cell capacitors during the series operation. When there are five capacitors in, the resonant tank is formed by five capacitors in series with L_s. When there are four capacitors in, the resonant tank is formed by four capacitors in series with L_s. Therefore, two resonant frequencies exist in the operation. Furthermore, for a general converter, the resonant frequency in the negative half-cycle is written as

$$f_{rn} = \frac{1}{2\pi\sqrt{L_s C/N}}. \tag{7}$$

The resonant frequency in the positive half-cycle is

$$f_{rp} = \frac{1}{2\pi\sqrt{L_s C/(N-1)}}. \tag{8}$$

As $f_{rp} < f_{rn}$, f_{rp} and f_{rn} are defined as the first resonant frequency and the second resonant frequency, respectively. The resonant tank waveforms of the proposed converter when using an operating frequency between f_{rp} and f_{rn} are shown in Fig. 6. Here, a low dc current plus an ac current on the parallel inductor are assumed. Note that this converter is operating differently to the classic LLC resonant converters [22] as two resonant frequencies exist during an operation cycle. In the case of Fig. 6, as in the positive half-cycle $f_e > f_{rp}$, the series current resonates with frequency of f_{rp} and the converter operates in the CCM. In the negative half-cycle $f_e > f_{rn}$, the series current resonates with frequency of f_{rn} and the converter operates in the DCM. There are five operating cycles in each switching cycle. Therefore, based on Fig. 6, the voltages and currents of the two switches in any cell can be obtained in Fig. 7. Note that when a switch is OFF, the current is zero. It can be seen that the converter can achieve ZCS and ZVS for the upper switches, but it cannot achieve soft switching for the lower switches. The turn-off current of the lower switch is high because the operating frequency is higher than the second resonant frequency f_{rn}. In general, ZCS cannot be achieved for any switch if the operating frequency is higher than the second resonant frequency f_{rn}. On the other hand, if the operating frequency is lower than the first resonant frequency f_{rp}, ZCS and ZVS for upper switches and near ZCS and near ZVS for lower switches are achieved.

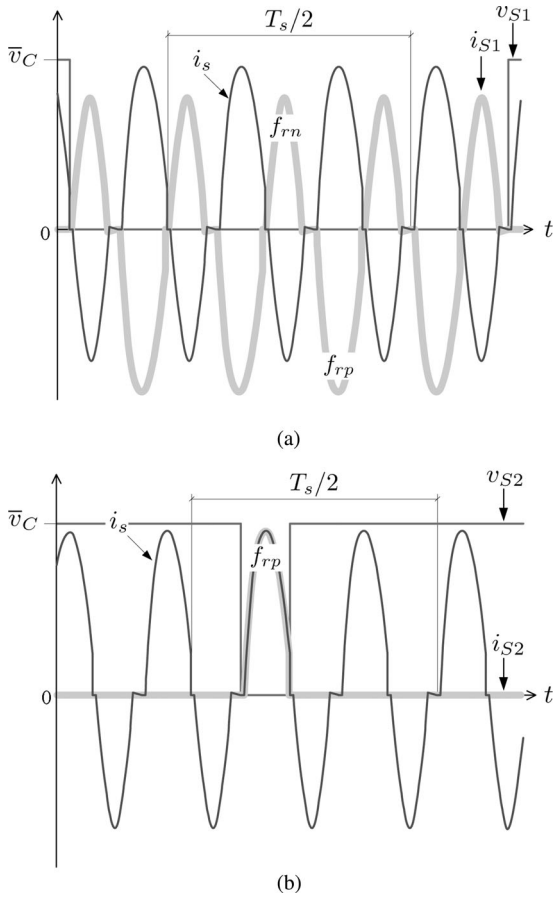

Fig. 7. Time-domain waveforms of the voltages and currents of the cell switches. (a) Upper switch. (b) Lower switch.

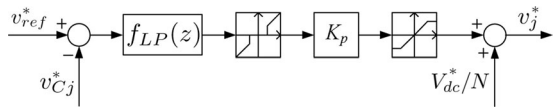

Fig. 8. Voltage controller of each cell.

However, the low operating frequency results in high conducting peak current. For most IGBTs, as both the collector–emitter saturation voltage and diode forward voltage increase significantly if the current increases, higher peak current may lead to higher conduction losses. Meanwhile, the stress on devices is also increased. On the other hand, when the switching frequency increases, switching losses will increase significantly due to the increased times of switching actions. Therefore, a good tradeoff according to a practical converter should be made to minimize the total losses.

Note that the resonant operation with inherent-balancing of the converter is achieved using a diode rectifier. Thus, the converter topology can only provide unidirectional power flow. The bidirectional operation may be achieved using an active rectifier instead. However, as an active rectifier has three different voltage levels on its ac input side, implementing active voltage clamping for cell capacitor balancing is difficult. This converter topology would require a new control scheme and a different operation method.

TABLE I
PARAMETERS OF THE TWO CONVERTER SCHEMES

Scheme	Side	Device voltage	Device current	Module number	IGBT/Diode applicable
ISOP DAB	Input	2000 V	10 A	5	5SNG 0250P330305×10
	Output	800 V	25A	5	DSEP60-12AR×20
Proposed	Input	2223 V	125 A	5	5SNG 0250P330305×10
	Output	800 V	125 A	1	DSEP60-12AR×20

III. IMPLEMENTATION AND APPLICATIONS

To implement a converter prototype, digital signal processors can be used as the main controller for measuring feedback signals and generating phase-shifted PWM signals. As explained in the previous section, the proposed converter has an inherent-balancing ability. Therefore, the converter can operate under the open-loop condition without using balancing control. However, active balancing control methods can still be used to ensure proper operation under certain circumstances. The performances of the converter with and without balancing control will be compared in the next section.

A. Balancing Control

Fig. 8 shows the balancing controller of the proposed converter. In order to balance the capacitor dc voltages, measuring the capacitor voltage of each cell is required. The reference voltage $v^*_{\rm ref}$ for each cell is calculated from the averaged voltage of the capacitors, which is expressed as

$$v^*_{\rm ref} = \frac{1}{N}\sum_{j=1}^{N} v^*_{Cj}. \tag{9}$$

As the cell capacitors are in the resonant operation, each capacitor voltage contains a considerable ac component. First-order low-pass filters are used to obtain the dc components of the capacitor voltages. As low-pass filters have to be implemented digitally, the transfer function of the filter can be written as

$$f_{\rm LP}(z) = \frac{\alpha}{z-1+\alpha} \tag{10}$$

with $\alpha = \omega_c T_b$, where ω_c is the cutoff angular frequency and T_b is the sampling period.

By comparing the reference voltage to the dc voltage of each cell, a proportional feedback control is used for regulation. A dead zone is created to allow a small tolerance of voltage imbalance. A saturation is used to limit the adjustable duty-ratio range. As the series current is positive at each switching instant (or in average), current measurement is not necessarily required for voltage balancing. The capacitor voltage can be charged by increasing the duty ratio of each cell slightly.

B. Step-Down DC Transformer

The proposed converter has inherent-balancing ability and therefore can operate using open-loop control. Regardless of the voltage drop of semiconductors and tolerance of the cell components, the ideal output voltage is proportional to the input voltage when the switching frequency is fixed. This gives the possibility of using the proposed converter as a dc transformer. The ratio between the output voltage and the input voltage is roughly determined by the number of cells. By increasing the number of cells, higher step-down ratio can be achieved. However, as explained in the previous section, the current stress will be further increased as a function of N. To achieve higher step-down ratio, isolation transformers can be used to increase the step-down ratio without increasing the series ac current. The topology in Fig. 1(c) is recommended for higher step-down ratio dc–dc conversions.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SYSTEM

Symbol	Quantity	Value
P	Rated power	250 W
V_{dc}	Nominal input dc voltage	500 V
v_o	Output dc voltage	45 V
I_{pk}	Maximum switch current	30 A
T_b	Sampling period	1 ms
L_{in}	Input filter inductor	9.8 mH
C_{in}	Input filter capacitor	840 μF
L_s	Series inductor	6.5 μH
L_p	Parallel inductor	3.3 mH
C_1	Cell 1 capacitor	57.9 μF
C_2	Cell 2 capacitor	69.1 μF
C_3	Cell 3 capacitor	58.2 μF
C_4	Cell 4 capacitor	57.7 μF
C_5	Cell 5 capacitor	57.8 μF
C_o	Output capacitor	3 mF

C. Output Voltage Regulator

If the switching frequency is limited in a certain range for a practical application, the proposed converter may require a secondary dc–dc conversion stage to regulate the output voltage. This is a good solution for output voltage control. However, classic frequency controllers can be used for output voltage regulation without a secondary dc–dc converter. Frequency controllers have limitations in many applications, but as a simple solution, they can achieve the requirement under some certain circumstances.

D. Economic Analysis Example on Low-Power Application

This section shows an example of the real value of the proposed concept. The generally used the input-series-output-parallel (ISOP) converter scheme with dual active bridges (DAB) is compared with the proposed converter scheme based on medium-voltage and low-power applications from the economic point of view. Both systems operate as step-down dc–dc converters from 10 kV to 800 V with a power rating of 100 kW. For the ISOP converter, there are five series half-bridge modules on the input side and five parallel diode bridge modules on the output side connected via five isolation transformers. In contrast, the proposed converter has five series half-bridge modules on the input side and one diode bridge on the output side. To implement the converters, the parameters of the modules of the two converter schemes are listed in Table I.

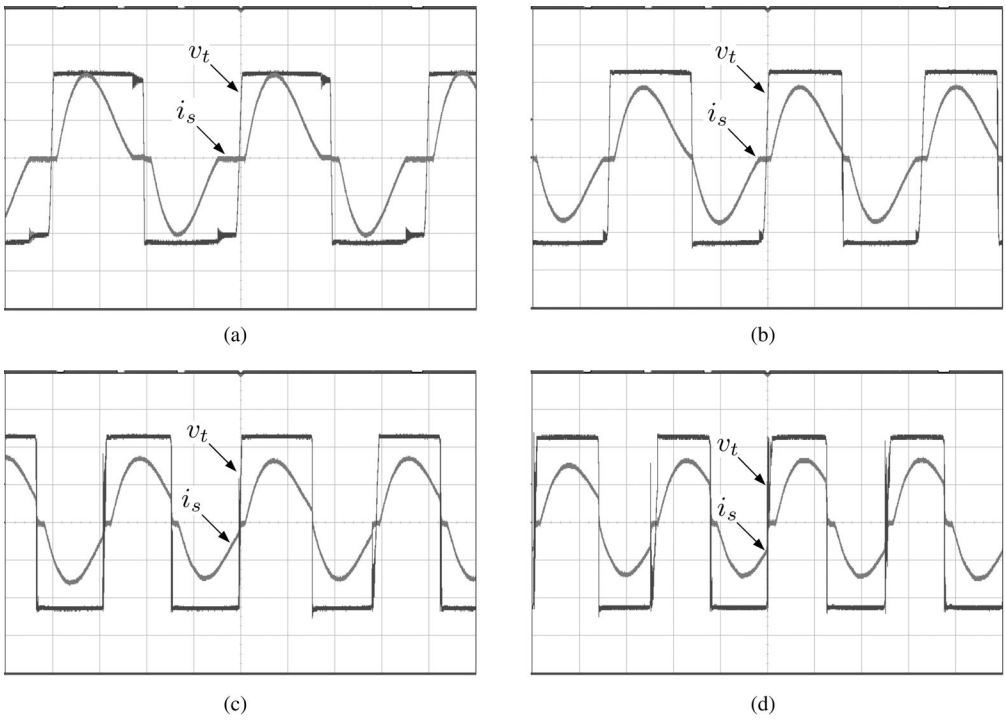

Fig. 9. Experimental waveforms under the open-loop condition (X–axis: Time, 20 μs/div, Y–axis: Magnitude of the rectifier input voltage: 20 V/div, and series current: 5 A/div) with (a) 2.5 kHz switching frequency. (b) 3 kHz switching frequency. (c) 3.5 kHz switching frequency. (d) 4 kHz switching frequency.

As the input voltage is 10 kV, with five modules used, each module should withstand voltage of more than 2 kV. The ABB HiPak IGBT half-bridge modules 5SNG 0250P330305, which can withstand 3.3 kV dc voltage are used. The current rating of each module is 250 A, which is the lowest current available in 3.3 kV HiPak product series. The output side in both schemes has a voltage of 800 V and a total current of 125 A (equivalent to five parallel diodes with 25 A in each). Therefore, IXYS diodes (DSEP60-12AR) with the ratings of 1200 V and 60 A can be used. Compared to the cost of IGBTs, the cost of diodes is almost negligible. The ISOP DAB scheme uses five HiPak IGBT modules with 10 A current flowing through each device, but the proposed scheme uses five HiPak IGBT modules with around 125 A current flowing through each device. The currents in both schemes are small enough compared to the 250 A device rating. Both schemes use the same numbers of semiconductor devices. On the other hand, the ISOP DAB scheme requires several bulky, heavy, and costly isolation transformers. Hence, for this low-power (100 kW) application example, the proposed scheme exhibits obvious predominance compared to the ISOP DAB scheme in terms of cost and economy. However, for high-power applications, the device current of the proposed converter will be much higher and IGBTs with high-current rating are required. Under such condition, the proposed converter will not be economic and efficient. It may be practical for high-power applications in the future if the ratings of semiconductors are improved and the price is reduced. Compared to the ISOP DAB scheme, the proposed scheme has higher losses and higher device cost on the input voltage side. Nevertheless, the proposed converter does not require isolation transformers withstanding the entire input high voltage and operates with much higher frequency reducing the sizes of passive components. There is one centralized rectifier used on the low-voltage output side. As a result, with the possibilities of semiconductor cost reduction, it provides a further option of implementing a high step-down ratio dc-dc converter comparable to traditional ISOP converters.

IV. Test Results

An experimental prototype was constructed based on the proposed circuit in Fig. 3 with five half-bridge cells. The dc supply was rated at 500 V. Between the dc supply and the converter stack, an input LC filter was connected to suppress the ac current going to the dc supply. The filter inductance and capacitance were selected as 9.8 mH and 0.84 mF, respectively. The half-bridge cells were implemented using capacitors with nominal capacitance value of 45 μF and IGBTs with PWM deadband of 5.3 μs. Note that big tolerance of capacitance applies during the manufacturing process. As a result, real values of the cell capacitors are different from each other. The switching frequency for each cell was chosen ranging from 2 to 4 kHz. Therefore, the operation frequency range was from 10 to 20 kHz. The nominal series resonant inductance was 4 μH and the parallel inductance was 3.3 mH. The capacitance of the output filter was 3 mF. The detailed circuit parameters are listed in Table II.

A. Open-Loop Tests

Four typical switching frequencies were used for open-loop tests. The basic operation of the proposed circuit was tested without balancing control or feedback control. The input dc voltage was 500 V. The proposed circuit has two different resonant frequencies f_{rp} and f_{rn}. With roughly measured parameters in Table II, the two resonant frequencies can be calculated as $f_{rp} = 16.8$ kHz and $f_{rn} = 18.8$ kHz, respectively. Note that

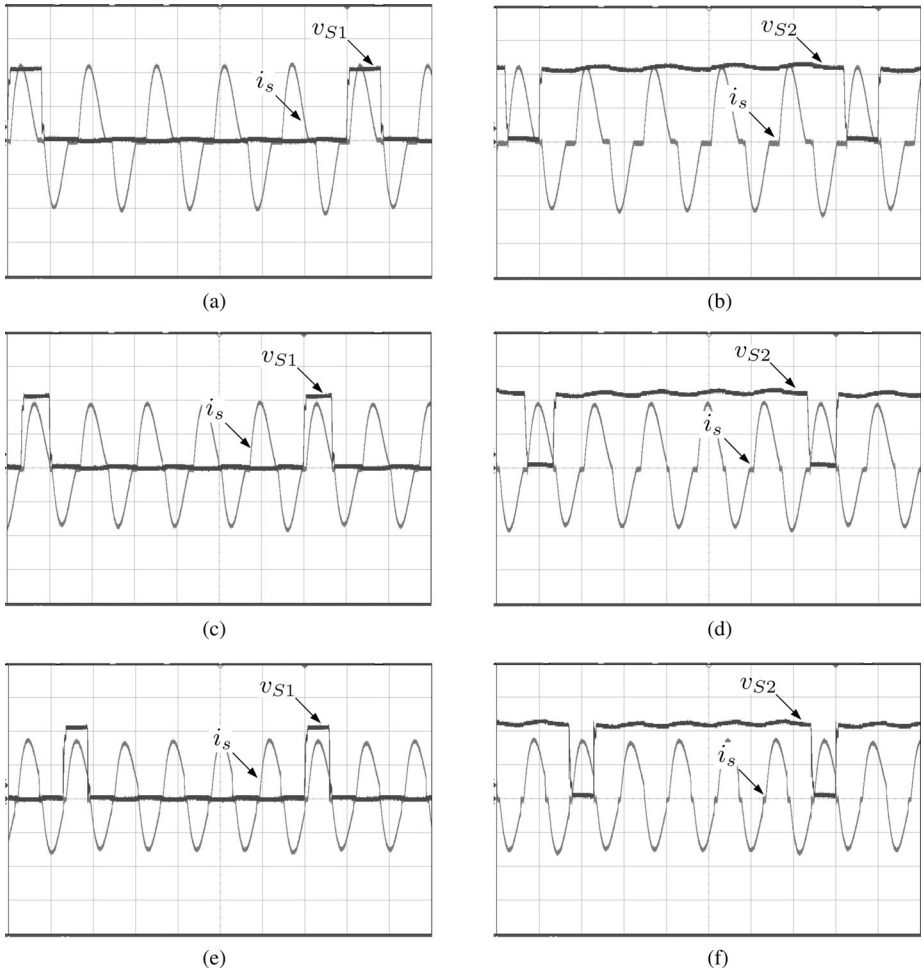

Fig. 10. Experimental waveforms of switch voltages in Cell 1 under the open-loop condition (X–axis: Time, 50 μs/div, Y–axis: Magnitude of the cell switch voltage: 50 V/div, and series current: 5 A/div) (a) Upper switch voltage with 2.5 kHz switching frequency. (b) Lower switch voltage with 2.5 kHz switching frequency. (c) Upper switch voltage with 3 kHz switching frequency. (d) Lower switch voltage with 3 kHz switching frequency. (e) Upper switch voltage with 3.5 kHz switching frequency. (f) Lower switch voltage with 3.5 kHz switching frequency.

the real resonant frequencies may be slightly different from the estimated values. However, this does not affect the operation principle of the converter. To show the typical waveforms, operating frequencies were chosen as 12.5, 15, 17.5, and 20 kHz to verify the design and analysis.

Fig. 9 shows the open-loop controlled experimental waveforms of the rectifier input voltage and series current. When the equivalent operation frequency is smaller than both f_{rp} and f_{rn}, the series current resonates quickly and the rectifier input current becomes zero before both the ends of positive half-cycle and negative half-cycle. The converter is fully operating in the DCM [see Fig. 9(a)]. If the operating frequency is increased close to the first resonant frequency f_{rp}, the rectifier input current becomes zero at the end of the positive half-cycle [see Fig. 9(b)]. However, as this operating frequency is still smaller than the second resonant frequency f_{rn} in the negative half-cycle, the rectifier input current becomes zero before the end of the negative half-cycle, which can be observed in Fig. 9(b). Similarly, if the operating frequency is increased close to the second resonant frequency f_{rn}, it becomes higher than the first resonant frequency f_{rp}. The key waveforms can be seen in Fig. 9(c). In the positive half-cycle of Fig. 9(c), the series current resonates slower than the operating frequency and the converter operates in the CCM. However, the rectifier input current reaches zero at the end of the negative half-cycle. The last experimental waveform in Fig. 9(d) shows that when the operating frequency is higher than both f_{rp} and f_{rn}, the converter operates in the CCM during both positive half-cycle and negative half-cycle. Under this condition, the series current peak is much smaller than that of the previous results and the stress on switches is much lower, but the turn-off currents of switches become much higher.

The voltages applied on the upper switch and the lower switch of a cell can be observed in Fig. 10. When the upper switch is ON and the lower switch is OFF, the voltage on the upper switch is almost zero and the voltage on the lower switch is almost the cell capacitor voltage. Meanwhile, the cell capacitor is in the series resonant operation. Therefore, during this period, the voltage on the lower switch contains a higher ripple. On the contrary, when the upper switch is OFF and the lower switch is ON, the voltage on the upper switch is almost equal to the cell capacitor voltage and the voltage on the lower switch is almost zero. During this period, the cell capacitor is out of the series resonant operation, and the voltage on the upper switch should be constant. It can be seen from Fig. 10(a), (c), and (e) that the upper switch off-time

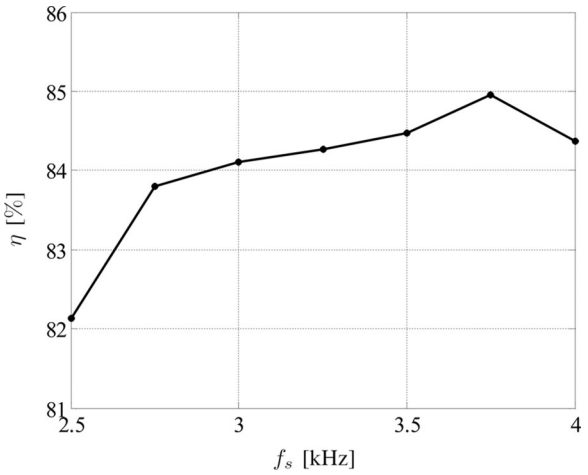

Fig. 11. Efficiency versus switching frequency.

ripple is smaller than that of the lower switch in Fig. 10(b), (d), and (f). Comparing Fig. 10(e) and (f) to Fig. 7, it can be seen that the theoretical waveforms and the experimental waveforms are in good agreement.

The efficiency of the converter versus the switching frequency is shown in Fig. 11. The results were obtained under the same input voltage condition (500 V). It can be observed from the experimental results that the maximum efficiency is achieved when the switching frequency is over 3.5 kHz. Although the turn-off current [see Fig. 10(f)] is higher than that with lower switching frequencies [see Fig. 10(b) and (d)], the peak current is significantly reduced. Lower conduction losses are therefore achieved resulting in lower total losses.

Furthermore, the efficiency was tested under open-loop conditions with a wide input voltage range. The results are shown in Fig. 12(a). It can be seen that low switching frequency reduces the efficiency slightly, as the conduction losses are the main component of power losses. With the increased input voltage, the efficiency can be significantly improved. This is due to the voltage drop on switches that does not increase as quickly as the output voltage does. The typical collector–emitter saturation voltage and diode forward voltage of the IGBTs we used are 1.8 and 2.5 V, respectively. Furthermore, improvement of efficiency by using dc power supplies with higher voltage or IGBTs with lower saturation voltage and lower forward voltage may be a possible solution.

The output dc voltage is changing almost proportionally to the input dc voltage, which can be observed in Fig. 12(b). It means the proposed converter can be used as a dc transformer with good linearity. The ideal ratio of the output dc voltage to input dc voltage should be $1/(2N-1) = 0.11$. As the switches have voltage drop and deadband, the conversion ratio is lower than the theoretical value. However, with a good linearity, the proposed converter can still behave as a dc transformer if the parameters are preadjusted according to the specification.

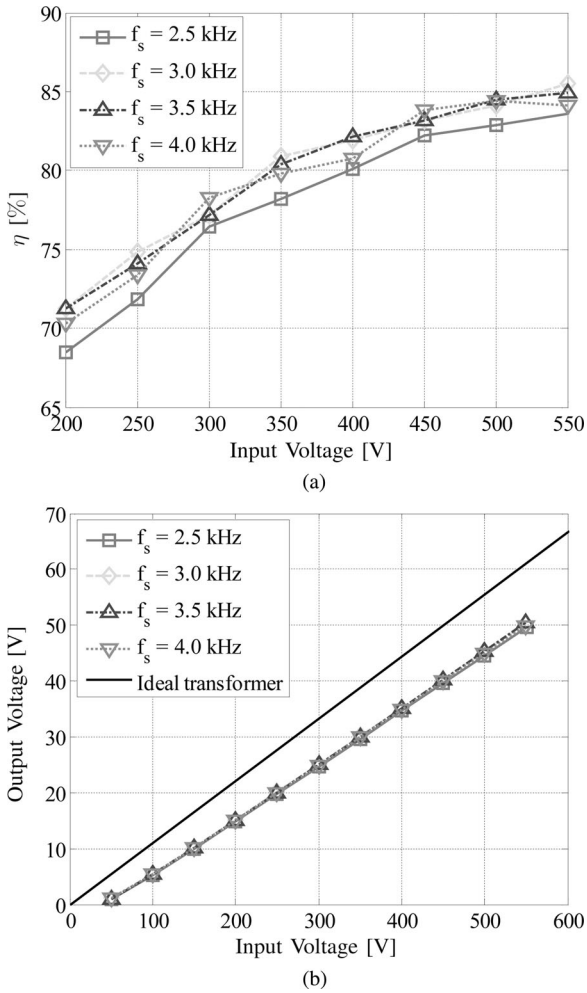

Fig. 12. Experimental results with the variable input voltage. (a) Efficiencies versus input voltage. (b) Output voltages versus input voltage.

B. Closed-Loop Tests

The closed-loop controller proposed in the previous section was implemented digitally. The converter was tested with a variable input dc voltage. The experimental results of a closed-loop capacitor balancing were compared to open-loop test results. It can be seen from Fig. 13 that without balancing control, the capacitor voltages of the converter are naturally balanced. In some applications, voltage sensors can even be eliminated from the converter for low-cost purposes. However, balancing control can be used to suppress the differences between the capacitor voltages.

With closed-loop balancing control and frequency control, the experimental waveforms of the rectifier input voltage and series current are shown in Fig. 14. Note that the conduction losses are considerable when frequency changes, the output voltage regulation function is based on the open-loop experimental test results. When the input voltage changes, it can be seen that the frequency has been adjusted to maintain the output voltage around the rated value (45 V). To show the output voltage regulation, Fig. 15 compares the output voltage of closed-loop tests with that of open-loop test results. It is shown that when the frequency controller is used, the output voltage changes slightly

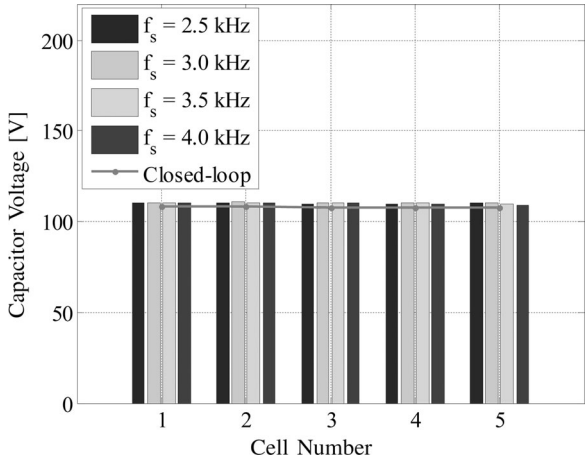

Fig. 13. Comparison of capacitor voltages between the closed-loop controller and open-loop controller.

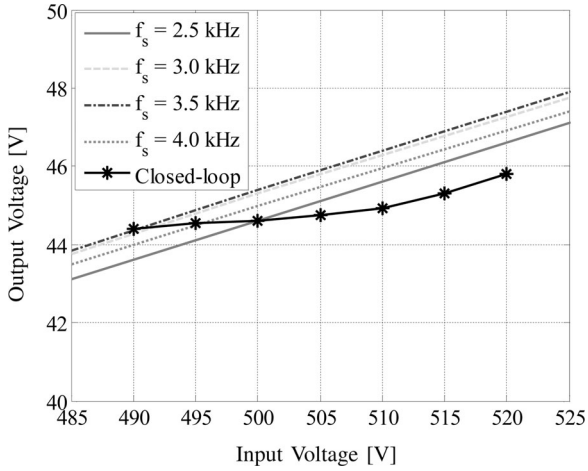

Fig. 15. Output voltage regulation of closed-loop controller.

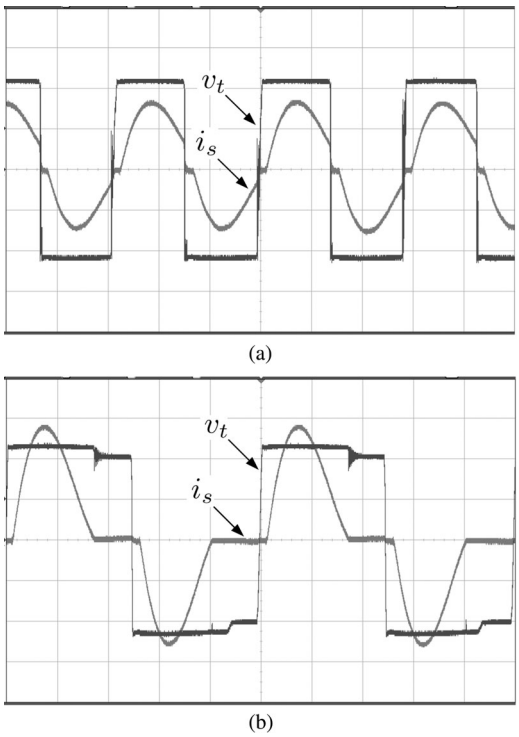

Fig. 14. Experimental waveforms under the closed-loop condition (X–axis: Time, 20 μs/div; Y–axis: Magnitude of the rectifier input voltage: 20 V/div; and series current: 5 A/div) with (a) 480 V input voltage. (b) 520 V input voltage.

around the rated output voltage value. To achieve a more accurate output voltage for a wide input range, a lower ratio between L_p and L_s should be used. However, this may increase the maximum parallel current i_p. A trade-off between output voltage regulation and power losses can be made to determine the inductance ratio [23]. A secondary converter can also be used to regulate the voltage level. The frequency–voltage regulator of the proposed converter is only a simple solution suitable for some certain applications.

It is worth mentioning that the experimental tests were arranged simply to verify a concept design. For an input voltage of 500 V, the proposed converter is not the best solution. The proposed converter may be more useful for high-voltage applications where the modular multilevel configuration is necessary. For a practical application, detailed sizing and system design need to be considered [29]. Moreover, further studies need to be done on the balance between the cost and performance. The proposed converter should be carefully designed and compared to other options. The converter scheme used in practice should be chosen depending on applications to obtain a good tradeoff from the economic point of view.

V. Conclusion

As high step-down ratio dc–dc converters become increasingly interesting, there is a strong demand of novel dc–dc converter topologies. This paper has presented a new transformerless MMC dc–dc converter. The dc capacitors of the cells are used also for the resonant operation. The equivalent operating frequency can be increased as a function of the number of half-bridge cells and the voltage step-down ratio is also dependent on the number of the cells. The proposed converter has a simple configuration and inherent-balancing capability. Two resonant operating frequencies exist in the converter. The converter can operate under open-loop control as a dc transformer. It exhibits a good linearity with different switching frequencies. When the closed-loop controller is used for the converter, the capacitor voltages are balanced and the output voltage is regulated within a smaller tolerance range of the rated value. Compared to the other topologies such as PETs, the proposed converter may exhibit more losses as a high ac current is flowing through the cells. However, the proposed converter can eliminate the use of transformers and even cell voltage sensors. Hence, the proposed converter has the feature of reliability, scalability, and simplicity which may be suitable for high-voltage and low-power applications.

Acknowledgment

The authors would like to thank Dr. R. Silversides who provided extensive support during the experimental tests.

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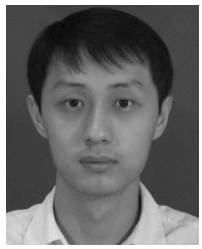

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